AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A computer system comprising:

a chipset including a bus-IO controller, a memory controller and a first video controller integrated into the chipset;

a second video controller coupled to the chipset;

a display device coupled to the video controllers;

a low-resistance switching device included in the chipset configured to receive video signals from either of the video controllers at respective inputs and to selectively provide the signals to a compatible display device; and

the switching device being coupled to a connector for the display device;

whereby only the second video controller provides its video signals to the switching device through the chipset via an AGP port.

2. (Cancelled).

3. (Cancelled).

4. (Cancelled)

5. (Cancelled).

6. (Previously Presented) The computer system of claim 1, further comprising:

a processor coupled to the chipset; and

a system memory configured to store a program that is executable by the processor;

wherein the program includes instructions for causing the switching device to selectively provide the signals to the display device.

7. (Cancelled).

8. (Cancelled).

9. (Previously Presented) The computer system of claim 1, wherein the signals include analog and digital signals.

10. (Previously Presented) A computer system comprising:

a chipset including a bus-I/O controller, a memory controller and a first video controller integrated into the chipset;

an interface coupled to the chipset and configured to receive a second video controller coupled to the chipset;

a display device coupled to the video controllers;

a low-resistance switching device included in the chipset coupled to receive video signals from either of the video controllers at respective inputs and to selectively provide the signals to a compatible device; and

the switching device being coupled to a connector for the display device;

whereby only the second video controller provides its video signals to the switching device through the chipset via an AGP port.

11. (Cancelled).

12. (Cancelled).

13. (Cancelled).

14. (Cancelled).

15. (Previously Presented) The computer system of claim 10, further comprising:

a processor coupled to the chipset; and

a system memory configured to store a program that is executable by the processor;

wherein the program includes instructions for causing the switching device to selectively provide a signal from the first video controller to the display device in response to the second video controller not being coupled to the interface, and wherein the program includes instructions for causing the switching device to selectively provide a signal from the second video controller to the display device in response to the second video controller being coupled to the interface.

16. (Cancelled).

17. (Cancelled).

18. (Previously Presented) The computer system of claim 10, wherein the signals include analog and digital signals.

19. (Cancelled).

20. (Cancelled).

21. (Currently Amended) A method of providing a video signal to a display device in a scalable platform comprising:

providing a chipset including a bus-I/O controller, a memory controller and a first video controller integrated into the chipset;

providing a second video controller coupled to the chipset;

providing a display device coupled to the video controllers;

configuring a low-resistance switching device included in the chipset to receive video signals at respective inputs from either of the video controllers and to selectively provide the signals to a compatible display device; and

the second video controller only providing its video signals to the switching device through the chipset via an AGP port.